# 20EC2106 - DIGITAL LOGIC DESIGN & COMPUTER ORGANIZATION

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| Course Category: |  Program Core | Credits: | 3 |
| Course Type: | Theory | Lecture-Tutorial-Practical: | 3-0-0 |
| Prerequisite: | Basic knowledge in identifying components, structure and internals of a computer. | Sessional Evaluation:Univ. Exam Evaluation:Total Marks: | 4060100 |
| Objectives: | * To learn about the number systems, gates to design digital circuits.
* To optimize circuits using gate level minimization.
* To design sequential and combinational logic systems.
* To understand the design of control unit, memory unit, I/O and Pipelining
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| Course Outcomes | Upon successful completion of the course, the students will be able to: |
| CO1 | Represent numbers in number systems and to perform primitive Boolean algebraic operations. |
| CO2 | Describe digital circuits and design Combinational circuits. |
| CO3 | Understand the Sequential Digital Systems and RTL concepts. |
| CO4 | Design a Basic Computer and know about different addressing modes. |
| CO5 | Understand the Control Mechanisms and Memory hierarchies. |
| CO6 | Acquire knowledge in I/O Organization and Parallel processing. |
| Course Content | UNIT-I**Digital Systems and Binary Numbers:** Digital Systems, Binary Numbers, Complements of Numbers, Signed Binary Numbers, Arithmetic Addition and Subtraction, Binary codes: Binary-Coded Decimal Code, Excess-3, Gray Code.**Boolean Algebra and Logic Gates:**Basic Definitions, Axiomatic definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Conversion of Canonical POS To Canonical SOP And Vice Versa.UNIT-II**Gate Level Minimization:**The Map method, Four Variable K-Maps. Products of Sum Simplification, Don’t – Care Conditions.**Combinational Logic:**Introduction, Analysis Procedure, Design Procedure, Binary Adder–Subtractor, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers.UNIT-III**Synchronous Sequential Logic:**Introduction to Sequential Circuits, Storage Elements: Latches, Flip-Flops**Registers and Counters:**Registers, Shift Registers, Ripple Counters, Synchronous Counters.UNIT-IV**Basic Computer Organization and Design**: Basic Structure of Computers, Data Representation, Instruction Codes, Computer Instructions, Instruction Cycle. **Central Processing Unit:** Instruction Formats, Addressing Modes, RISC, CISCUNIT-V**Micro programmed Control:** Control Memory, Address Sequencing, Design of Control Unit and Hardwired Control.**Memory System:** Memory Hierarchy, Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Cache Memories-Mapping Functions.UNIT-VI**Input-Output Organization:** Peripheral Devices, Input-Output Interface, Direct Memory Access.**Pipeline Processing:** Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline. |
| Text Books &ReferencesBooks | **TEXT BOOKS:**1. Digital Design –6th Edition, M.Morris Mano, Pearson Education/PHI.
2. Computer Organization – Carl Hamacher, Zvonko G. Vranesic, Safwat G. Zaky

**REFERENCE BOOKS:**1. Switching and Finite Automata Theory by Zvi. Kohavi, Tata McGraw Hill.
2. Switching and Logic Design, C.V.S. Rao, Pearson Education.
3. Digital Principles and Design – Donald D.Givone, Tata McGraw Hill, Edition.
4. Fundamentals of Digital Logic & Micro Computer Design, 5TH Edition, M. Rafiquzzaman John Wiley
5. Computer Organization and Architecture– William Stallings, 7th Edition.
6. Computer Organization and Design– P Paul Chowdary, 2rd Edition.
7. Computer Systems Design and Architecture – Vincent P and Harry F Jordan, 2nd Edition.
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| E-Resources | 1. <https://nptel.ac.in/courses>
2. <https://freevideolectures.com/university/iitm>
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**CO-PO Mapping:** 3-High Mapping, 2-Moderate Mapping, 1-Low Mapping, - -Not Mapping

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|   | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 3 | 2 | 3 | - |  | 2 | - | - | - | - | - | - |
| **CO2** | - | 2 | 2 | - | 2 | 1 | - | - | - | - | - | - |
| **CO3** | 3 | 2 | - | 2 | 3 | 3 | - | - | - | - | - | - |
| **CO4** | 1 | 2 | 2 | - | 3 | 3 | - | - | - | - | - | - |
| **CO5** | 3 | 2 | - | 2 | 2 | 1 | - | - | - | - | - | - |
| **CO6** | 3 | 2 | 2 | 1 | 2 | 2 | - | - | - | - | - | - |